FIG. 1

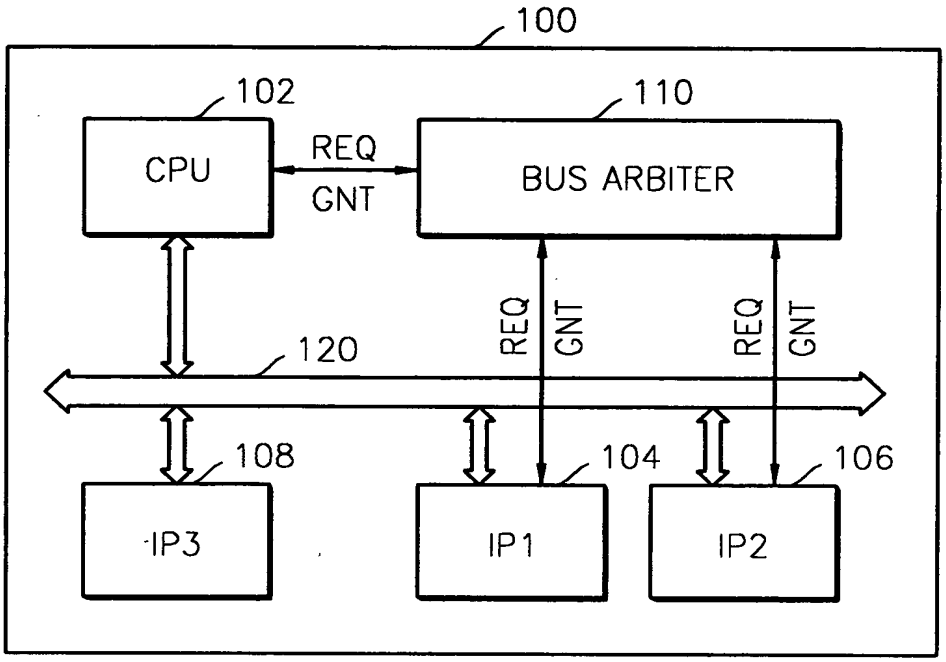

100
102
110
CPU
REQ
GNT
BUS ARBITER
120
REQ
GNT
REQ
GNT
108
104
106
IP3
IP1
IP2

FIG. 2

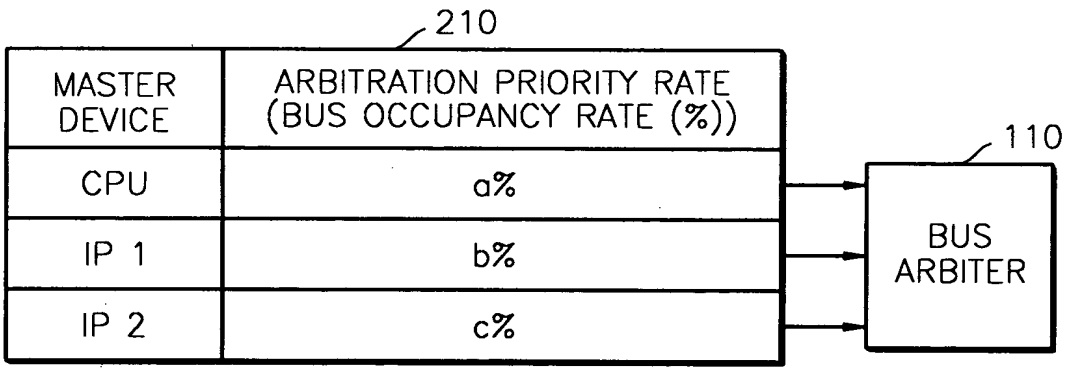

210
MASTER DEVICE
ARBITRATION PRIORITY RATE (BUS OCCUPANCY RATE (%))
CPU
a%
IP 1
b%
IP 2
c%
110
BUS ARBITER

FIG. 3

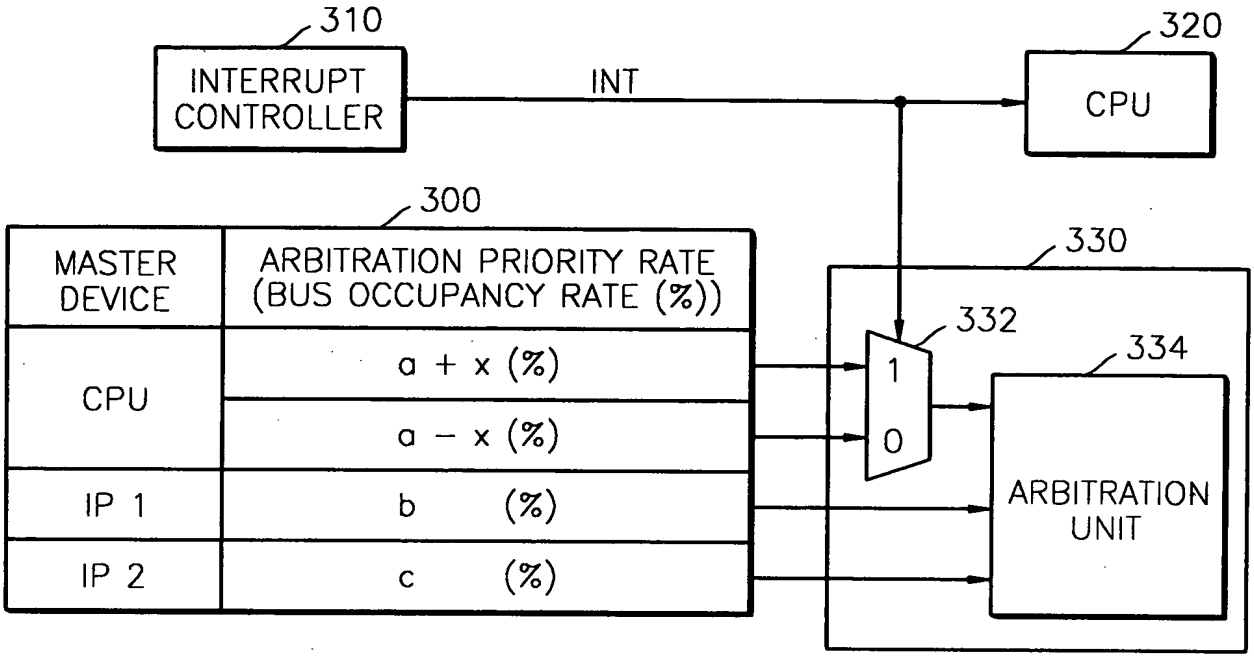

310
INTERRUPT CONTROLLER
INT
320
CPU
300
MASTER DEVICE
ARBITRATION PRIORITY RATE (BUS OCCUPANCY RATE (%))
CPU
a + x (%)
a − x (%)
IP 1
b (%)
IP 2
c (%)
330
332
1
0
334
ARBITRATION UNIT

FIG. 4

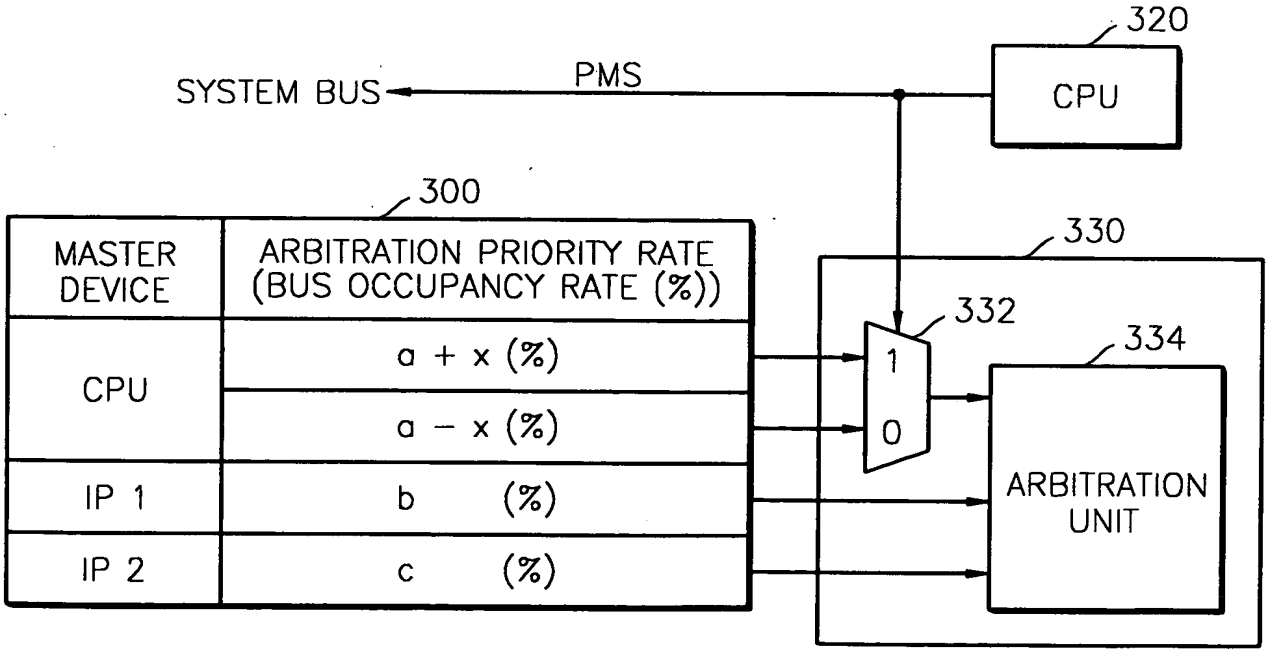

320
SYSTEM BUS
PMS
CPU
300
MASTER DEVICE
ARBITRATION PRIORITY RATE (BUS OCCUPANCY RATE (%))
CPU
a + x (%)
a − x (%)
IP 1
b (%)
IP 2
c (%)
330
332
1
0
334
ARBITRATION UNIT

FIG. 5

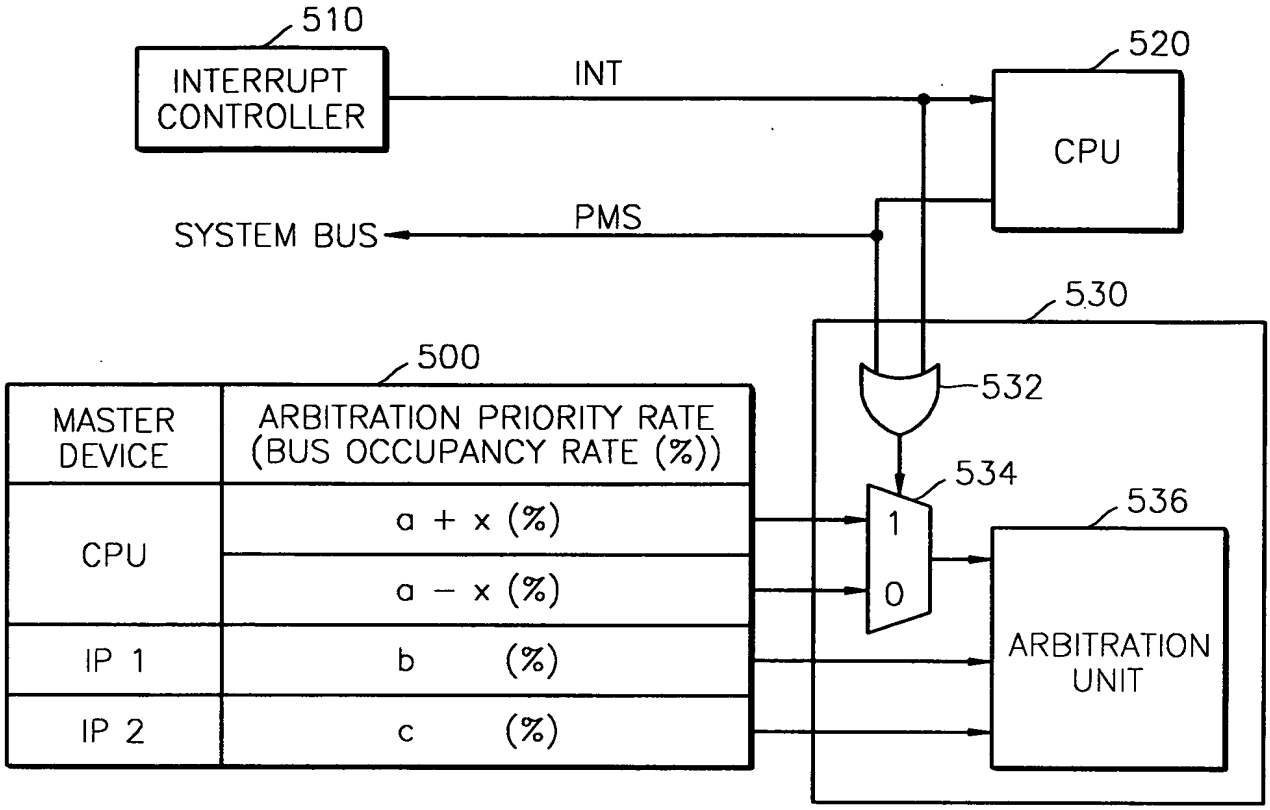

510
INTERRUPT CONTROLLER
INT
520
CPU
SYSTEM BUS
PMS
530
500
532
534
536
MASTER DEVICE
ARBITRATION PRIORITY RATE (BUS OCCUPANCY RATE (%))
CPU
a + x (%)
a − x (%)
IP 1
b (%)
IP 2
c (%)
1
0
ARBITRATION UNIT

FIG. 6

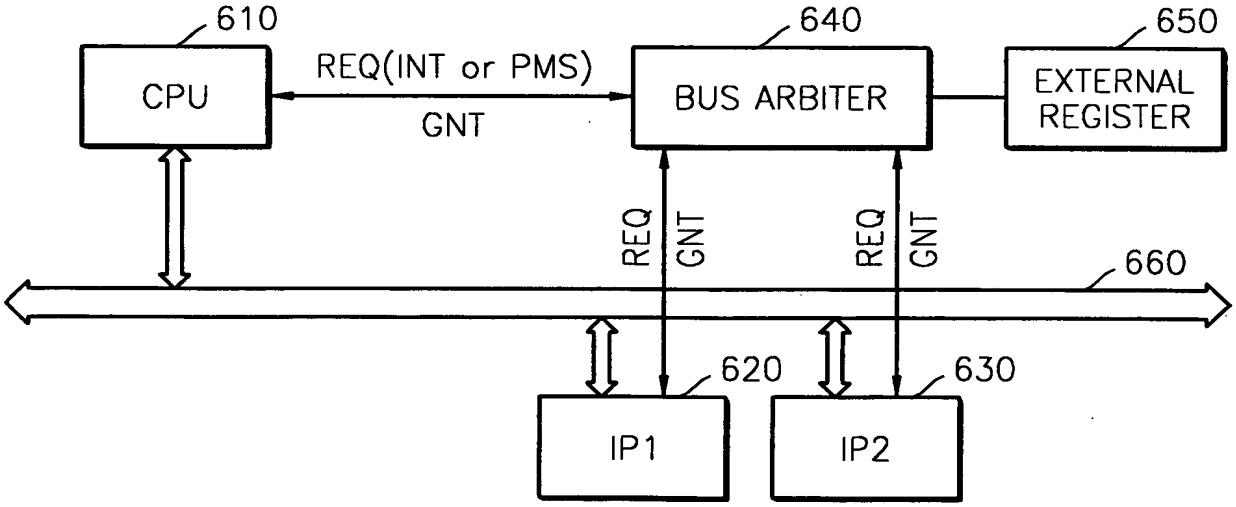

610
CPU
REQ(INT or PMS)
GNT
640
BUS ARBITER
650
EXTERNAL REGISTER
REQ
GNT
REQ
GNT
660
620
630
IP1
IP2

FIG. 7

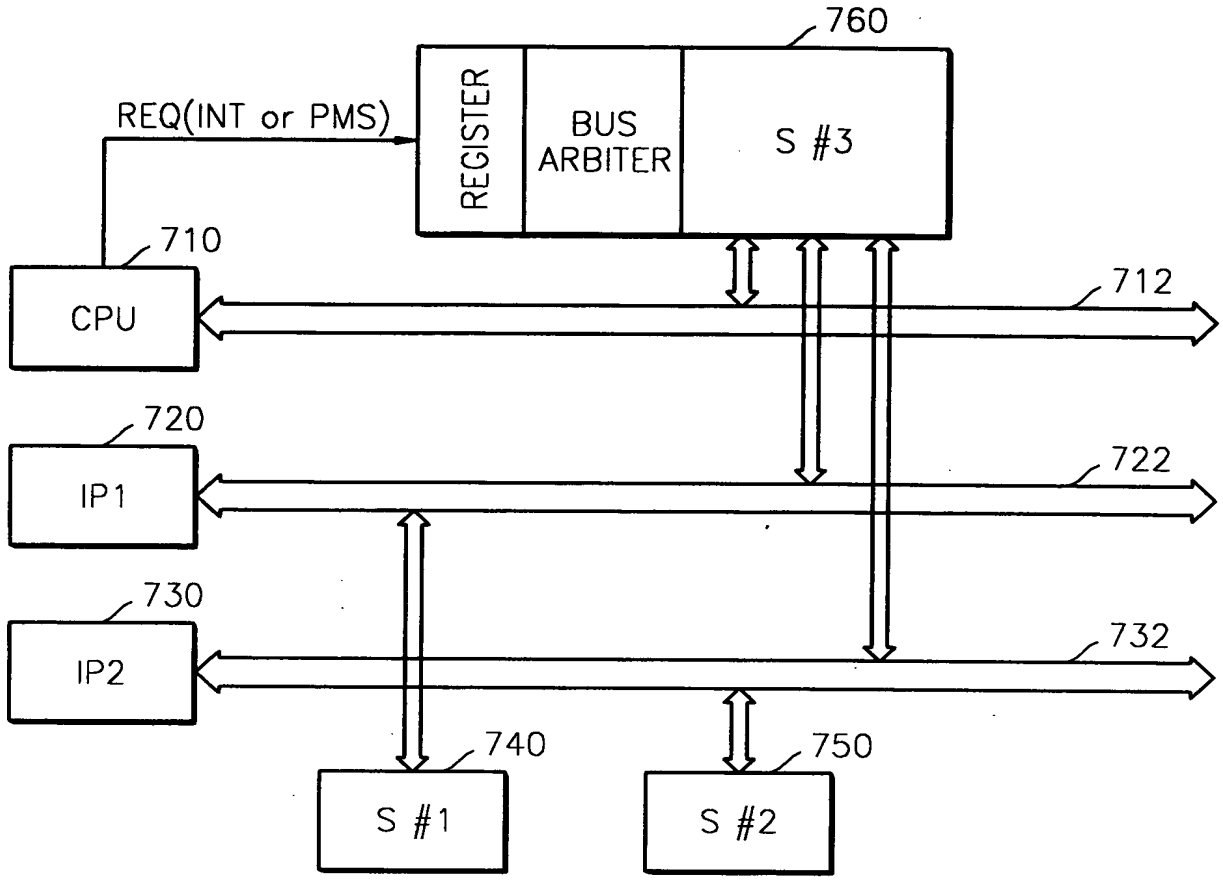
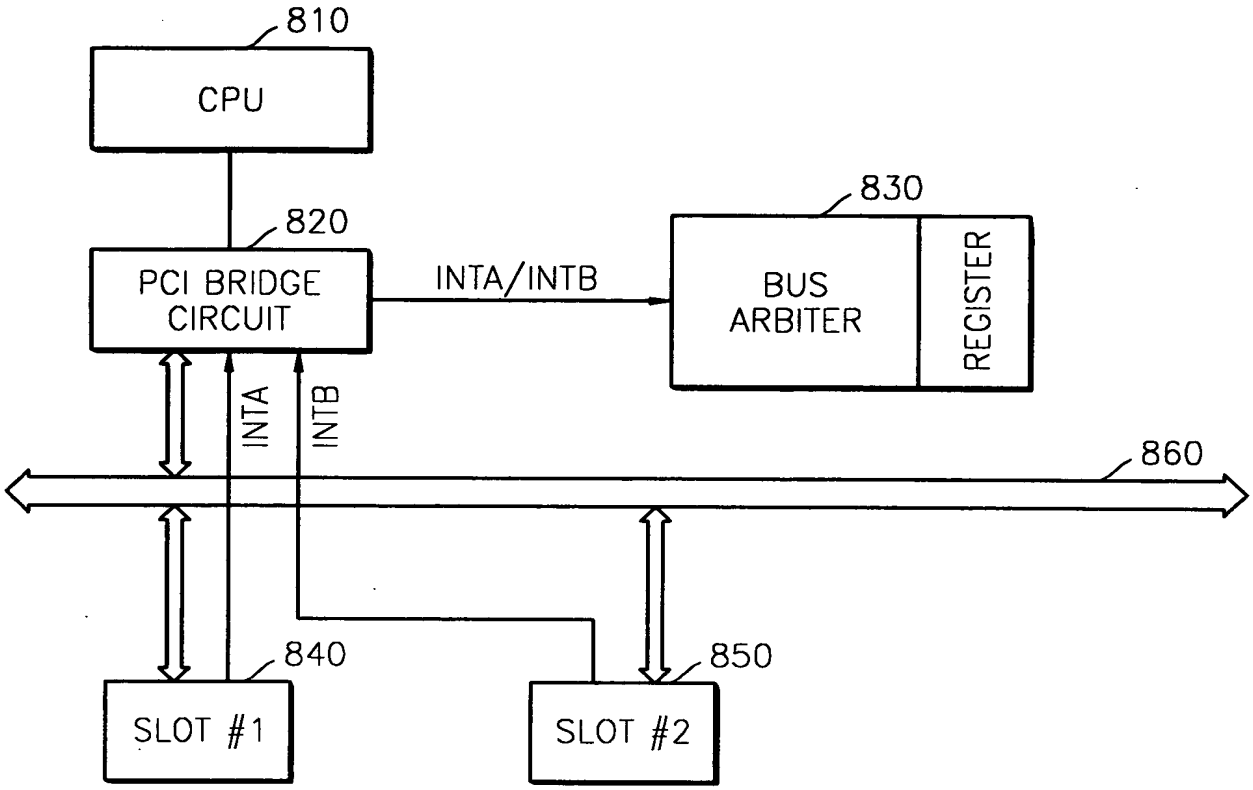

760
REGISTER
BUS ARBITER
S #3
REQ(INT or PMS)
710
CPU
712
720
IP1
722
730
IP2
732
740
S #1
750
S #2

FIG. 8


810
CPU
820
PCI BRIDGE CIRCUIT
INTA/INTB
830
BUS ARBITER
REGISTER
INTA
INTB
860
840
SLOT #1
850
SLOT #2